What is claimed is:

1. A non-volatile semiconductor memory device comprising:

a memory core circuit including a cell array in which electrically rewritable and non-volatile memory cells are arranged therein, decoders configured to select the memory cells, and sense amplifiers configured to perform data read and write of said cell array; and

a peripheral circuit including a memory controller configured to control data read and write in communication with said memory core circuit, wherein

said memory controller comprises:

an oscillator configured to generate an internal clock signal;

a timing control circuit configured to control timings of data read and write of said cell array as synchronous with said internal clock signal; and

a merge clock generation circuit configured to generate based on an external timing signal and said internal clock signal a merge clock signal serving for timing controlling a circuit portion in said peripheral circuit, said merge clock signal being defined as having a first signal period in which said external timing signal serves as a clock source and a second signal period without overlapping said first signal period, in which said internal clock signal serves as a clock source.

2. The non-volatile semiconductor memory device according to claim 1, wherein

said circuit portion includes an address circuit having an address register and address counter, and a command circuit configured to decode a command signal.

3. The non-volatile semiconductor memory device according to claim 1, wherein

said merge clock generation circuit comprises:

a first logic gate configured to draw said external timing signal to serve as said merge clock signal in said first

signal period under the control of an OR logic of an execute flag activating said timing control circuit and a synchronous execute flag generated by sampling said execute flag with said internal clock signal; and

a second logic gate configured to draw said internal clock signal to serve as said merge clock signal in said second signal period under the control of an AND logic of said execute flag and synchronous execute flag.

4. The non-volatile semiconductor memory device according to claim 1, wherein

said external timing signal includes write enable signal and read enable signal.

5. The non-volatile semiconductor memory device according to claim 1, wherein

said external timing signal includes write enable signal and read enable signal, and wherein

said merge clock signal generation circuit comprises a flip-flop which is set and reset by said write enable signal and read enable signal, respectively, to output an operation mode determining signal supplied to said circuit portion.

6. The non-volatile semiconductor memory device according to claim 3, wherein

said oscillator is configured to be activated by an OR logic of said execute flag and synchronous execute flag.

7. The non-volatile semiconductor memory device according to claim 1, wherein

said oscillator is configured to have an activation delay function for securing a clock blanking period between said first and second signal periods.

8. The non-volatile semiconductor memory device according to claim 3, further comprising

a combination logic circuit configured to set and reset said execute flag based on the operation states of said timing control circuit and said circuit portion.

9. The non-volatile semiconductor memory device according to claim 1, wherein

said cell array is formed of NAND cell units arranged therein, each NAND cell unit having plural memory cells connected in series.

10. An electric card equipped with a non-volatile semiconductor memory device, said device comprising:

a memory core circuit including a cell array in which electrically rewritable and non-volatile memory cells are arranged therein, decoders configured to select the memory cells, and sense amplifiers configured to perform data read and write of said cell array; and

a peripheral circuit including a memory controller configured to control data read and write in communication with said memory core circuit, wherein

said memory controller comprises:

an oscillator configured to generate an internal clock signal;

a timing control circuit configured to control timings of data read and write of said cell array as synchronous with said internal clock signal; and

a merge clock generation circuit configured to generate based on an external timing signal and said internal clock signal a merge clock signal serving for timing controlling a circuit portion in said peripheral circuit, said merge clock signal being defined as having a first signal period in which said external timing signal serves as a clock source and a second signal period without overlapping said first signal period, in which said internal clock signal serves as a clock source.

11. An electric device comprising:

a card interface;

a card slot connected to said card interface; and

an electric card defined in claim 10 and electrically connectable to said card slot.

12. The electric device according to claim 11, wherein said electric device is a digital still camera.